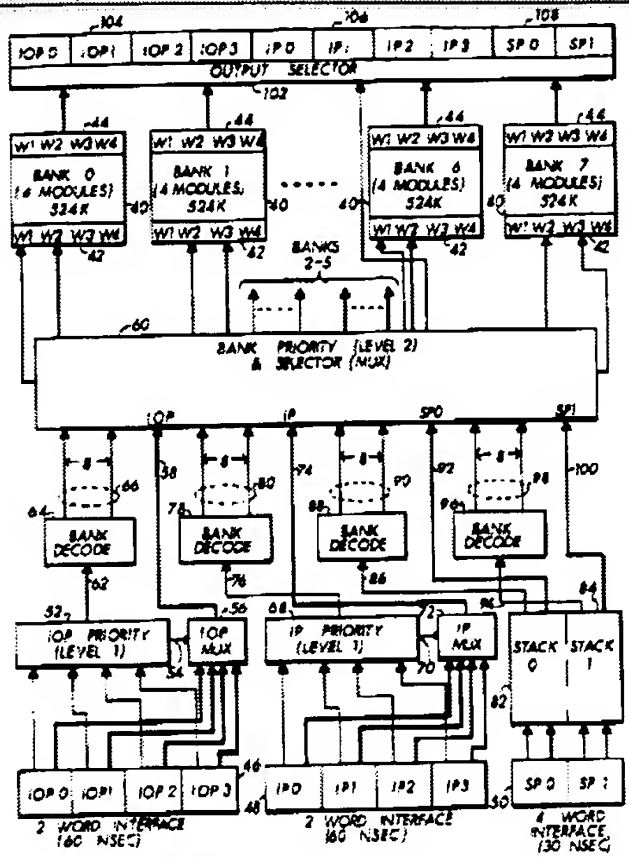

FIG. 2

EAST Browser | 4 (9) 2 and addres | US 6366524 B1 | Tag: S | Doc: 2/9 | Format: KWIC

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4 (9) 2 and addres | US 6366524 B1 | Tag: S | Doc: 2/9 | Forma

US-PAT-NO: 6366524

DOCUMENT-IDENTIFIER: US 6366524 B1

TITLE: Address decoding in multiple-bank memory architectures

---------- KWIC ----------

Abstract Text - ABTX (1):

Methods and apparatus for decoding an externally-applied address in a synchronous memory device are arranged to decode a first portion of the address during a setup time and to decode a second portion of the address following the setup time. The first portion of the address may be indicative of a bank address of a multiple-bank memory device. The second portion of the address may be indicative of row and column addresses within a bank of the multiple-bank memory device. Decoding of the first portion of the address is performed by an address input buffer stage having a decoder interposed between the input buffers and the address latches, such that the decoder generally replaces a delay stage of a typical input buffer stage. As such, the first portion of the address is decoded during a setup time. By decoding the first portion of the address during a setup time,

Details | Text | Image | HTML | KWIC

4 (9) 2 and addres | US 6366524 | Tag: S | Doc: 2/9 | "Full" 1/20 | Format

US006366524B1

United States Patent

Abedifard

(10) Patent No.: US 6,366,524 B1
(45) Date of Patent: Apr. 2, 2002

ADDRESS DECODING IN MULTIPLE-BANK MEMORY ARCHITECTURES

Inventor: Ebrahim Abedifard, Sunnyvale, CA (US)

Assignee: Micron Technology Inc., Boise, ID (US)

Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

Appl. No.: 09/615,197

Filed: Jul. 26, 2000

Int. Cl.[7] G11C 8/00

U.S. Cl. 365/230.06; 365/230.03; 365/230.08

Field of Search 365/230.06, 230.03, 365/230.06, 185.11

References Cited

U.S. PATENT DOCUMENTS

041,866	A	8/1991	Lee	
202,823	A *	4/1993	Shimogawa et al.	365/230.06
295,115	A *	3/1994	Furuya et al.	365/230.06
537,354	A	7/1996	Mochizuki et al.	
600,606	A	2/1997	Schaefer	
606,371	A	2/1997	Schaefer	
748,559	A *	5/1998	Kang	365/230.08
751,039	A	5/1998	Kaufman et al.	
787,457	A	7/1998	Miller et al.	
936,908	A	8/1999	Jeng et al.	
950,219	A *	9/1999	Rao	365/230.03
965,458	A	10/1999	Jeng et al.	
026,465	A	2/2000	Mills et al.	
157,578	A	12/2000	Kaufman et al.	
241,247	A	12/2000	Roohparvar et al.	
6,166,953	A *	12/2000	Yamazaki	365/230.03

OTHER PUBLICATIONS

Keeth, et al., "DRAM circuit design: a tutorial," IEEE Press, 2001, pp. 16–23, 142–153.

Micron Semiconductor Products, Inc., "2Mb, Smart 5 BIOS-Optimized Boot Block Flash Memory," *Flash Memory* www.micron.com, copyright 2000, Micron Technology, Inc., pp. 1–12.

Micron, "16 Mb: x16 SDRAM" *Synchronous DRAM*, www.micron.com, copyright 1999 Micron Technology, Inc., pp. 1–81.

* cited by examiner

Primary Examiner—Hien Hoang
(74) *Attorney, Agent, or Firm*—Fogg Slifer Polglaze Leffert & Jay, P.A.

(57) ABSTRACT

Methods and apparatus for decoding an externally-applied address in a synchronous memory device are arranged to decode a first portion of the address during a setup time and to decode a second portion of the address following the setup time. The first portion of the address may be indicative of a bank address of a multiple-bank memory device. The second portion of the address may be indicative of row and column addresses within a bank of the multiple-bank memory device. Decoding of the first portion of the address is performed by an address input buffer stage having a decoder interposed between the input buffers and the address latches, such that the decoder generally replaces a delay stage of a typical input buffer stage. As such, the first portion of the address is decoded during a setup time. By decoding the first portion of the address during a setup time, it is available to direct the second portion of the address to a proper decoder substantially without delay.

46 Claims, 8 Drawing Sheets

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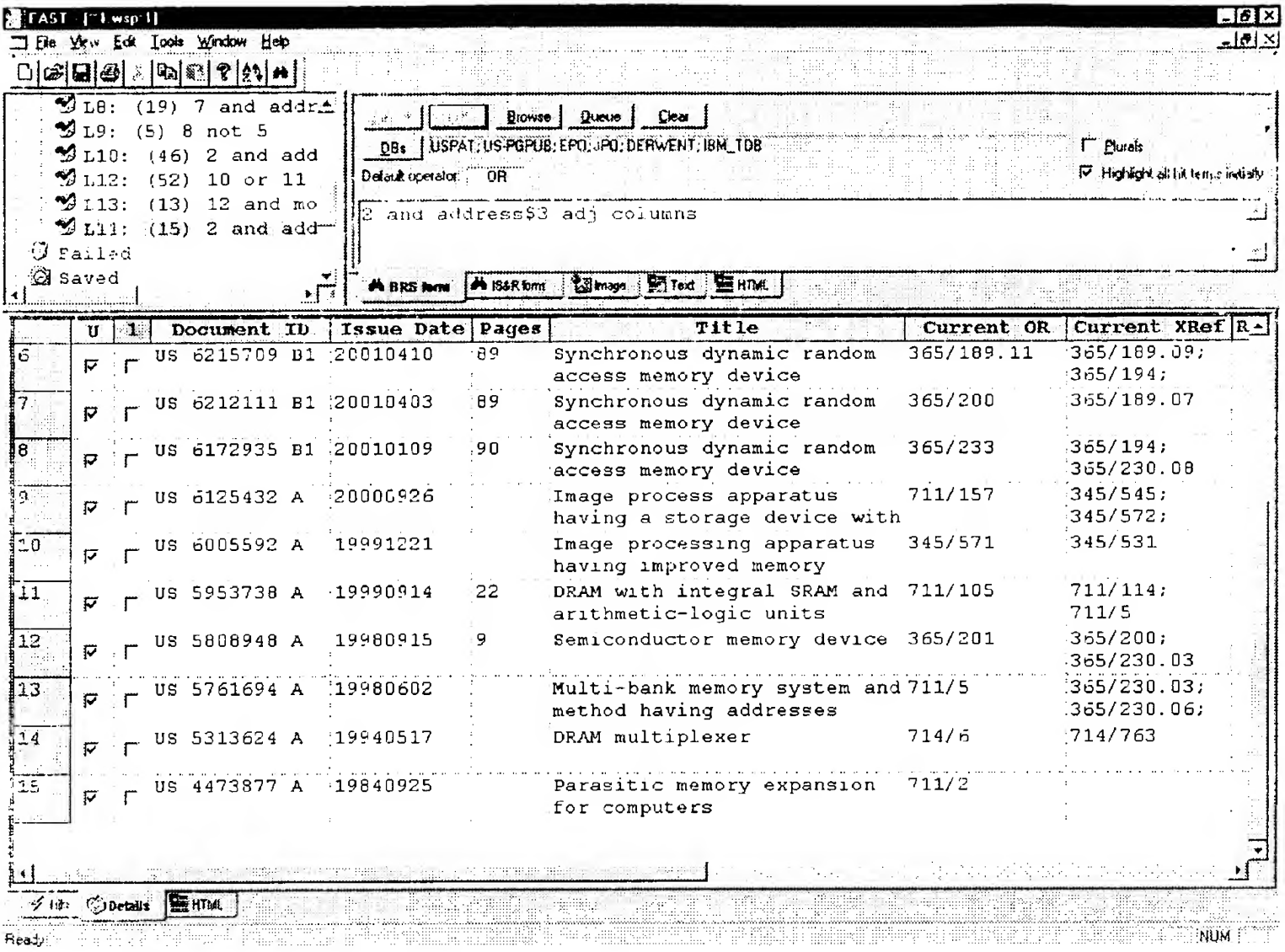

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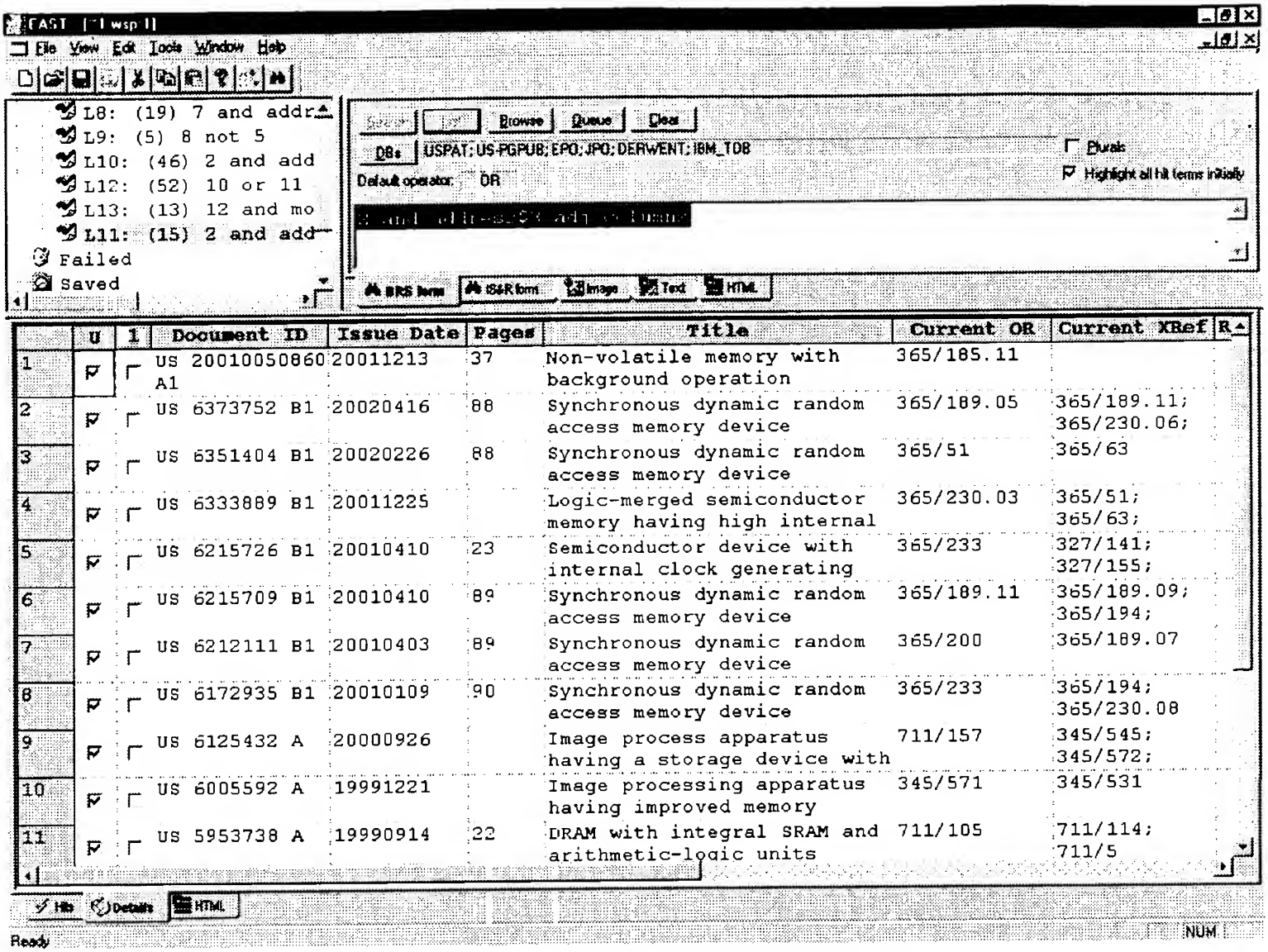
6	☑	☐	US 6215709 B1	20010410	89	Synchronous dynamic random access memory device	365/189.11	365/189.09; 365/194;	
7	☑	☐	US 6212111 B1	20010403	89	Synchronous dynamic random access memory device	365/200	365/189.07	
8	☑	☐	US 6172935 B1	20010109	90	Synchronous dynamic random access memory device	365/233	365/194; 365/230.08	
9	☑	☐	US 6125432 A	20000926		Image process apparatus having a storage device with	711/157	345/545; 345/572;	
10	☑	☐	US 6005592 A	19991221		Image processing apparatus having improved memory	345/571	345/531	
11	☑	☐	US 5953738 A	19990914	22	DRAM with integral SRAM and arithmetic-logic units	711/105	711/114; 711/5	
12	☑	☐	US 5808948 A	19980915	9	Semiconductor memory device	365/201	365/200; 365/230.03	
13	☑	☐	US 5761694 A	19980602		Multi-bank memory system and method having addresses	711/5	365/230.03; 365/230.06;	
14	☑	☐	US 5313624 A	19940517		DRAM multiplexer	714/6	714/763	
15	☑	☐	US 4473877 A	19840925		Parasitic memory expansion for computers	711/2		



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1	☑	☐	US 20010050860 A1	20011213	37	Non-volatile memory with background operation	365/185.11		
2	☑	☐	US 6373752 B1	20020416	88	Synchronous dynamic random access memory device	365/189.05	365/189.11; 365/230.06;	
3	☑	☐	US 6351404 B1	20020226	88	Synchronous dynamic random access memory device	365/51	365/63	
4	☑	☐	US 6333889 B1	20011225		Logic-merged semiconductor memory having high internal	365/230.03	365/51; 365/63;	
5	☑	☐	US 6215726 B1	20010410	23	Semiconductor device with internal clock generating	365/233	327/141; 327/155;	
6	☑	☐	US 6215709 B1	20010410	89	Synchronous dynamic random access memory device	365/189.11	365/189.09; 365/194;	
7	☑	☐	US 6212111 B1	20010403	89	Synchronous dynamic random access memory device	365/200	365/189.07	
8	☑	☐	US 6172935 B1	20010109	90	Synchronous dynamic random access memory device	365/233	365/194; 365/230.08	
9	☑	☐	US 6125432 A	20000926		Image process apparatus having a storage device with	711/157	345/545; 345/572;	
10	☑	☐	US 6005592 A	19991221		Image processing apparatus having improved memory	345/571	345/531	
11	☑	☐	US 5953738 A	19990914	22	DRAM with integral SRAM and arithmetic-logic units	711/105	711/114; 711/5	

FAST Browser - [13 (13) 12 and mode - US 6044032 | Tag: S | Doc: 9/13 | "Full" 2/16 (Total images 16)]

File Edit View Tools Window Help

[13 (13) 12 and mode - US 6044032 A | Tag: S | Doc: 9/13 | For

FAST Advanced Find

Find what: mode

Find Next | Cancel

Area: All / Sel/Cur — Direction: Up / Down — Match word: Whole / Left / Part / Right — Look in: Grid / Documents — Match case

rows in all of the banks 20 within the SDRAM 10. Examples of other well known commands include, but are not limited to, the ACTIVE, READ, WRITE, BURST TERMINATE, AUTO REFRESH, LOAD MODE REGISTER, COMMAND INHIBIT and NOP commands.

(13) The ACTIVE command is used to open up (or activate) a row of memory cells in a particular bank 20 for a subsequent access. The row remains active until a PRECHARGE command deactivates it. The READ command is used to initiate a burst read access for an active row. The WRITE command is used to initiate a burst write access for an active row. The READ and WRITE commands will also be accompanied with the column and bank addresses to complete the addressing for the command. The AUTO REFRESH command is used to refresh the contents of the memory arrays 20. The BURST TERMINATE command is used to truncate a read burst. The LOAD MODE REGISTER allows a mode register of the control circuit 12 to be loaded. The mode register contains information such as burst length and

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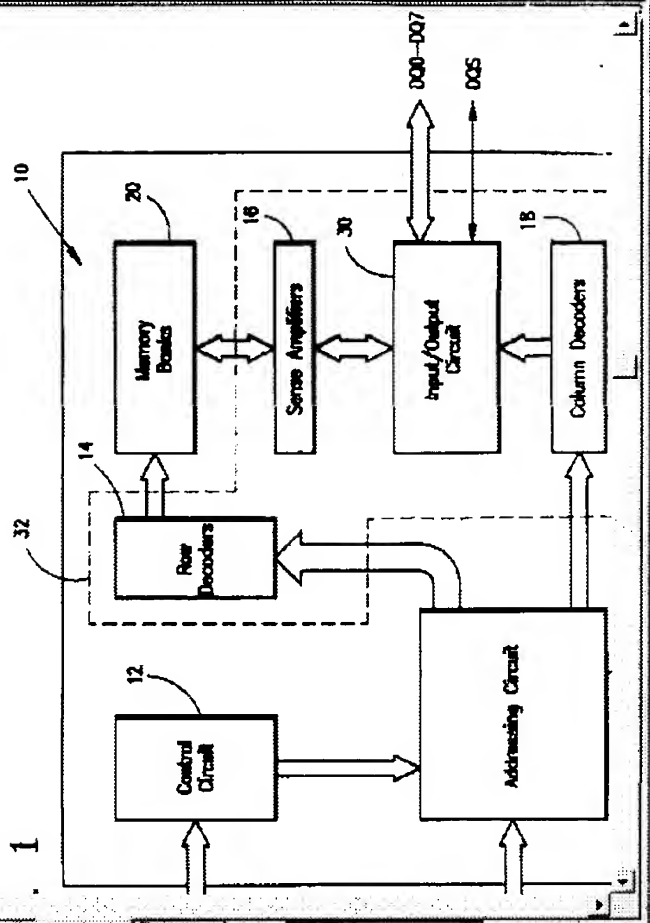
[13 (13) 12 and mode - US 6044032 | Tag: S | Doc: 9/13 | "Full" 2/16 (Tot



Details | Text | Image | HTML | Full

Ready

NUM

EAST Browser - [L9: (5) 8 not 5 | US 6111814 | Tag: S | Doc: 1/5 | "Full" 1/15 (Total images 15)]

File Edit View Tools Window Help

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Schaefer

[45] **Date of Patent:** *Aug. 29, 2000

[54] **SYNCHRONOUS DRAM MEMORY WITH ASYNCHRONOUS COLUMN DECODE**

[75] Inventor: **Scott Schaefer**, Boise, Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[*] Notice: This patent is subject to a terminal disclaimer.

[21] Appl. No.: **09/318,449**

[22] Filed: **May 20, 1999**

Related U.S. Application Data

[63] Continuation of application No. 08/926,946, Sep. 10, 1997 which is a continuation of application No. 08/772,976, Dec. 23, 1996, Pat. No. 5,721,859, which is a continuation of application No. 08/522,969, Sep. 1, 1995, Pat. No. 5,600,...

[51] **Int. Cl.**[7] **G11C 8/00**

[52] **U.S. Cl.** **365/233.5**; 365/230

[58] **Field of Search** 365/233.5, 233, 365/222, 230.08

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,719,602	1/1988	Hag	365/230
4,912,679	3/1990	Shirato	365/233.5
4,962,376	9/1990	Wang	365/233.5
4,972,374	11/1990	Wang	365/233.5
5,047,984	9/1991	Monden	365/233
5,179,535	1/1993	Nakayama	365/189.09
5,305,283	4/1994	Shimakura	365/230.08
5,327,394	7/1994	Green	365/233.5
5,414,673	5/1995	Ozaki	365/233.5
5,438,546	8/1995	Houston	365/227
5,659,507	8/1997	Yabe	365/222

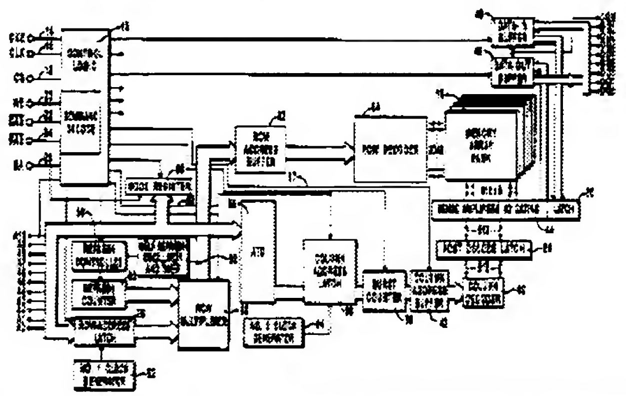
Primary Examiner—A. Zarabian

Attorney, Agent, or Firm—Workman, Nydegger & Seeley

[57] **ABSTRACT**

Disclosed is a synchronous DRAM memory module with control circuitry that allows the memory module to operate partially asynchronously. Specifically, a circuit is disclosed which utilizes address transition detection to begin decoding the column-address immediately after a new column-address is present on the address bus lines and without waiting for the column-address strobe signal to synchronize with the rising or falling edge of the synchronizing clock signal. Also disclosed is a manner of connecting the latching circuitry whereby each new column-address may be decoded and held within a buffer until the column-address strobe signal notifies the circuitry that the column-address is correct and is to be input into the microprocessor. Thus, each new column-address will be decoded immediately after it is present on the address lines and unwanted column-addresses will be discarded, while desired column-addresses are input into the memory array bank immediately upon the presence of the column-address strobe which denotes that the column-address is final. The present invention improves the access times of read and write operations in synchronous DRAM memory by up to a complete clock cycle.

46 Claims, 6 Drawing Sheets



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[75] Inventor: Yoshinori Okajima, Kawasaki, Japan

[73] Assignee: Fujitsu Limited, Kawasaki, Japan

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: 08/792,134

[22] Filed: Jan. 31, 1997

[30] Foreign Application Priority Data

Feb. 2, 1996 [JP] Japan 8-017990

[51] Int. Cl.[*] G06F 12/00

[52] U.S. Cl. 711/169; 711/5; 711/168, 711/167

[58] Field of Search 711/4, 5, 105, 711/106, 111, 147, 148, 149, 150, 151, 152, 167, 168, 170, 173

[56] References Cited

U.S. PATENT DOCUMENTS

4,633,434 12/1986 Scheuneman 364/900

5,384,745 1/1995 Konishi et al.

5,410,670 4/1995 Hasbun et al. .

5,737,563 4/1998 Shigeeda 395/405

5,745,418 4/1998 Ahrens et al. 365/230

5,748,914 5/1998 Barth et al. 395/285

5,768,559 6/1998 Lino et al. 395/484

FOREIGN PATENT DOCUMENTS

0 384 620A2 8/1990 European Pat. Off.

0 498 525A2 8/1992 European Pat. Off. .

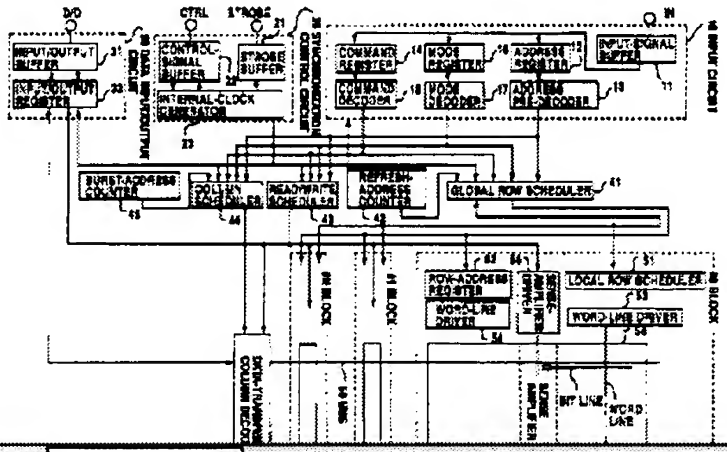
WO88/09995 12/1988 WIPO .

Primary Examiner—Eddie P. Chan
Assistant Examiner—Kimberly McLean
Attorney, Agent, or Firm—Nikaido, Marmelstein, Murray & Oram LLP

[57] ABSTRACT

A memory system using at least one DRAM chip and equipped with an interface for transferring input/output data in a packet format includes a plurality of banks within each of the at least one DRAM chip. The memory system further includes a control circuit for accessing a bank for data transfer of a given packet when the bank is different from a previous bank accessed for an immediately preceding packet, and for waiting for an operation to complete in the bank when the bank is the same as the previous bank.

6 Claims, 17 Drawing Sheets



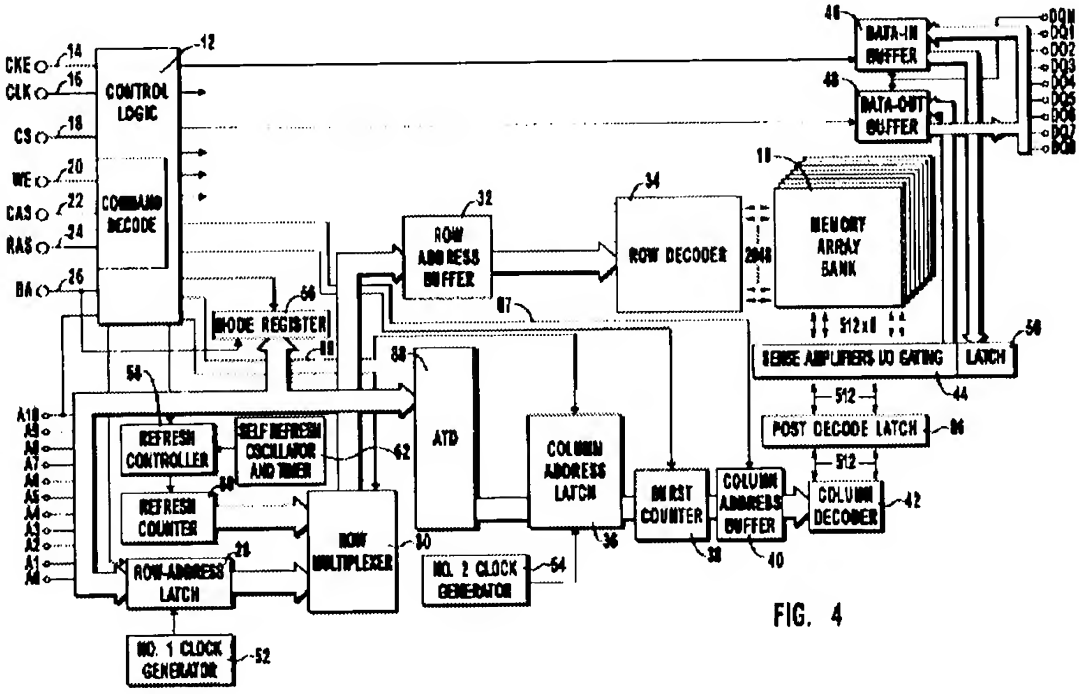


FIG. 4

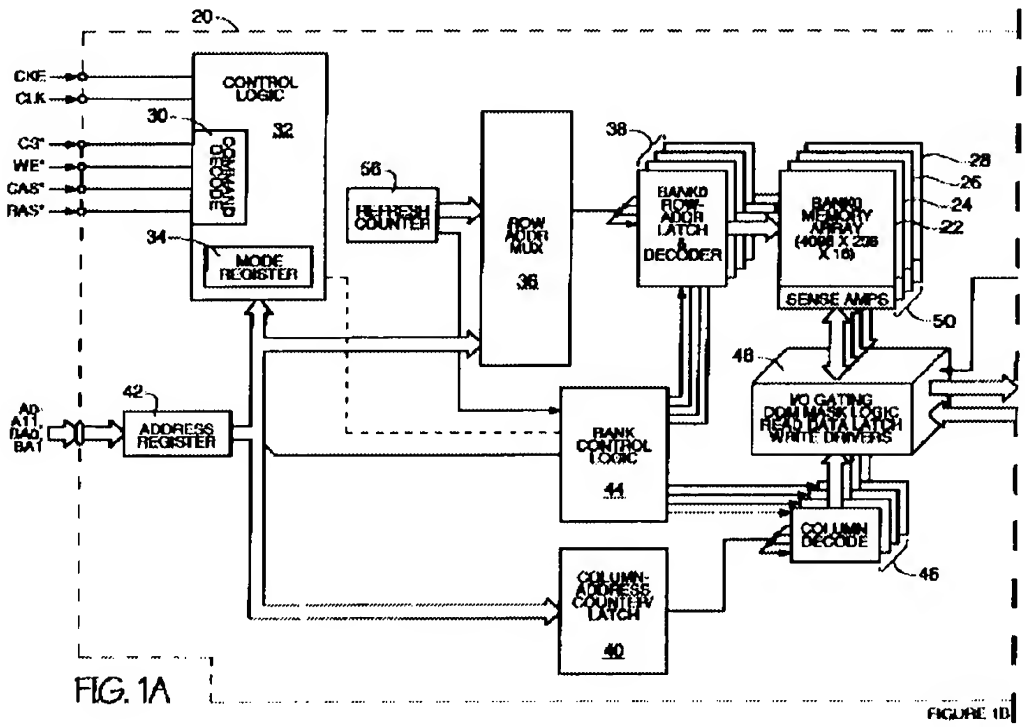
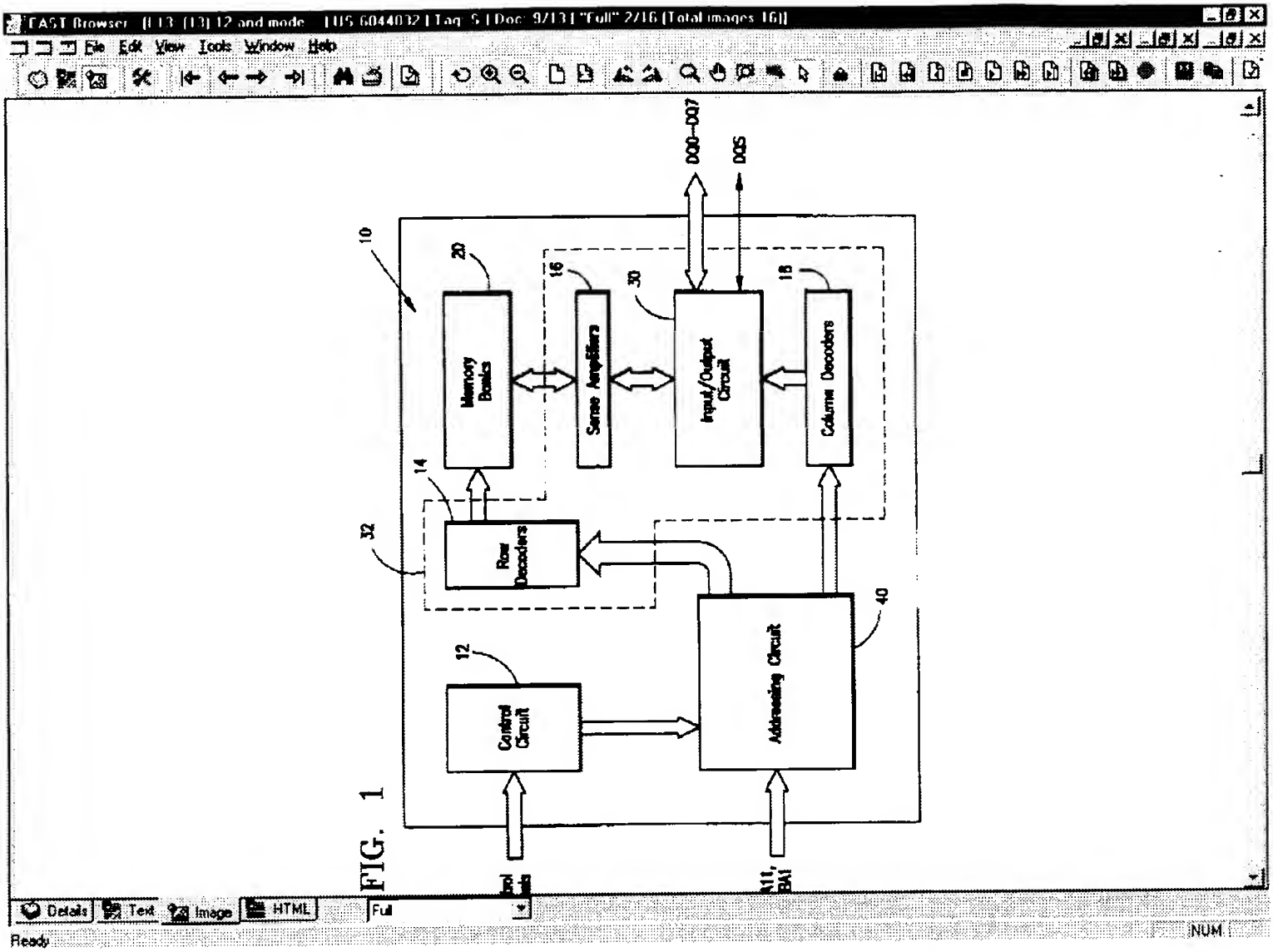


FIG. 1A

FIGURE 1B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10
20
16
30
18
Memory Banks
Sense Amplifiers
Input/Output Circuit
Column Decoders
14
32
Row Decoders
40
12
Control Circuit
Addressing Circuit

FIG. 1